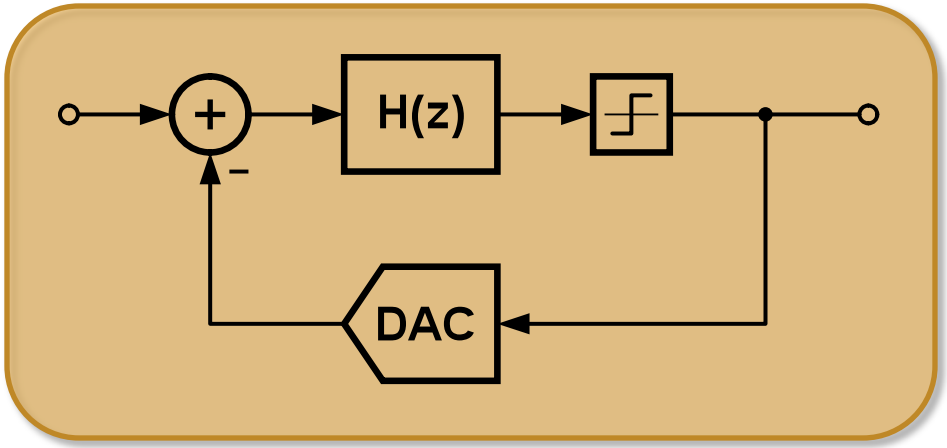
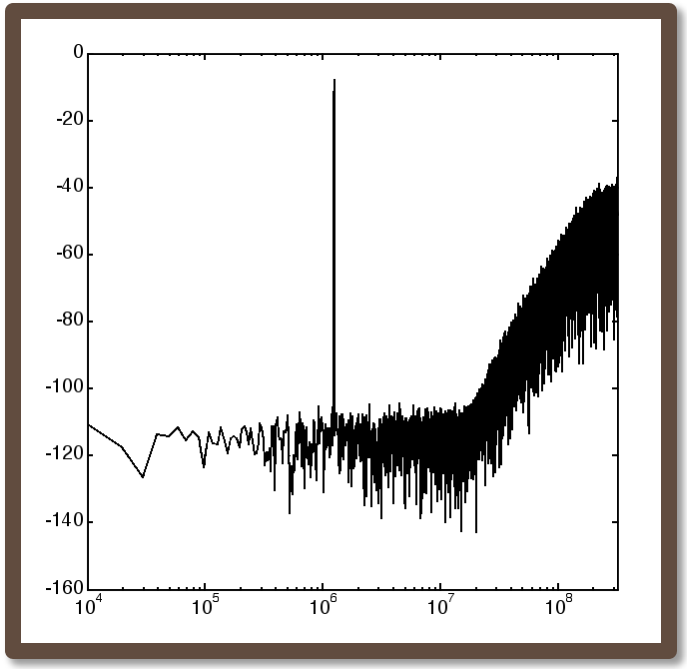




Brian L. Young, Oregon State University, 5/18/2009

ECE 627 PROJECT DESIGN STRATEGY

OUTLINE

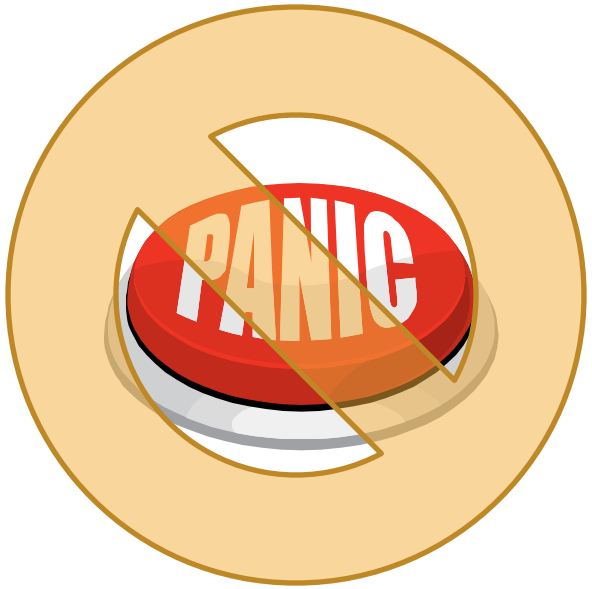
- Software Tools
- Preliminary Calculations
- Mathematical Design Script, MATLAB
- Simulink Modeling
- Circuit Implementation
- Simulink Results
- Suggestions

SOFTWARE TOOLS

- MATLAB/Simulink
- Delta Sigma Toolbox (MATLAB)
  - http://www.mathworks.com/matlabcentral/fileexchange/19
- SD Toolbox 2 (Simulink)
  - http://www.mathworks.com/matlabcentral/fileexchange/7589
- Cadence/Spectre
- SWITCAP (“sw2” on SunOS machine)

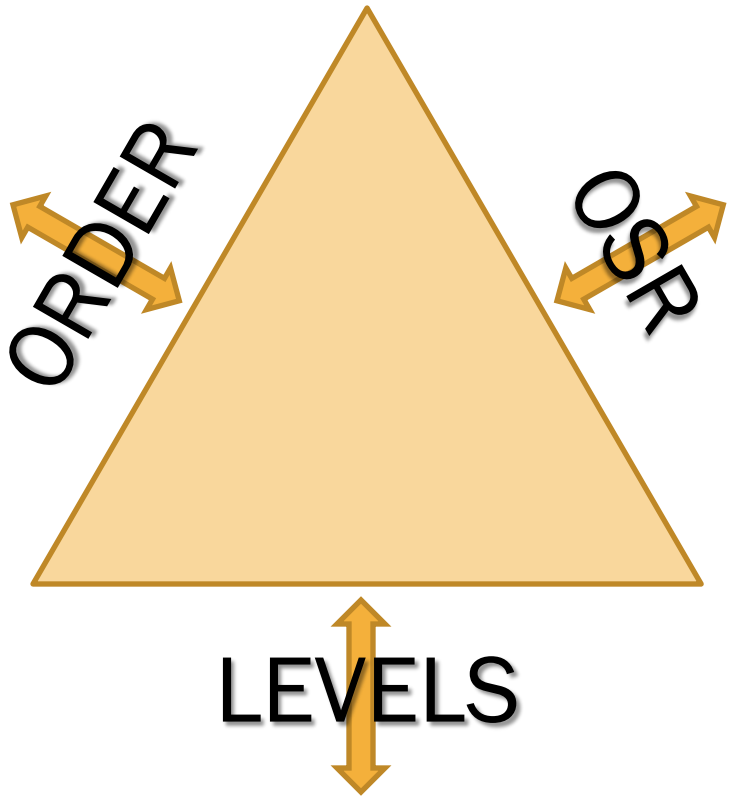
WHERE TO BEGIN

- *Panic* for 5 seconds…
- Now, Stop *Panicking*
- Examine Requirements
  - ENOB, F_{BW}, F_S, etc.
- Determine Target Technology
  - Same as ECE 626?
- Explore DStoolbox Demos
  - dsdemo[1-3,5].m



TRADEOFFS IN ΔΣ PARAMETERS

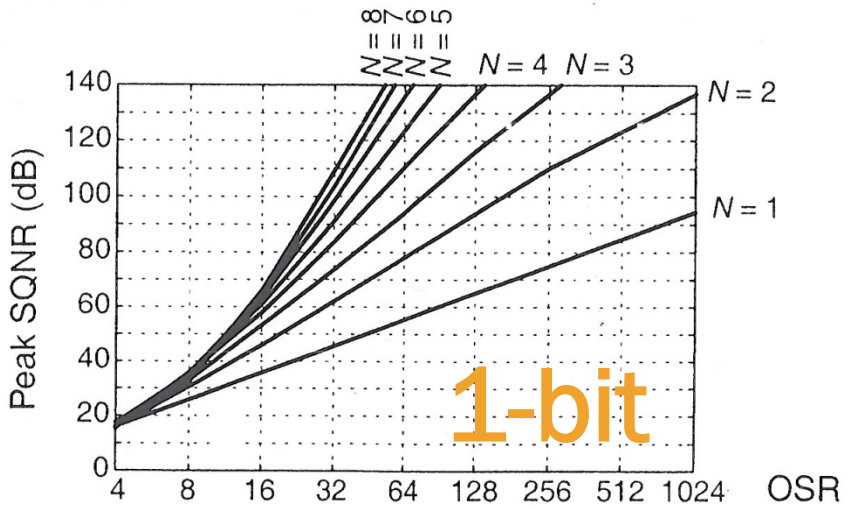
- Calculate SQNR
- Modulator Order, OSR, Quantizer Levels
- Power efficient designs → thermal noise limited, ~~quantization noise limited~~

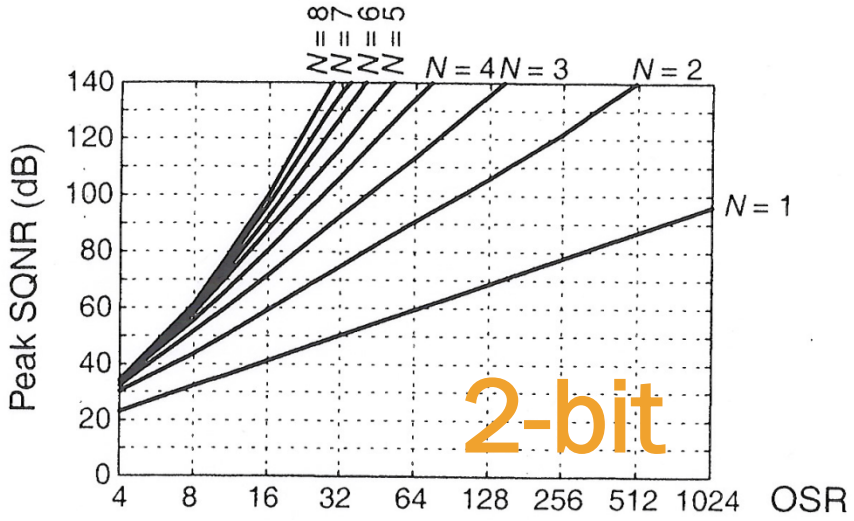


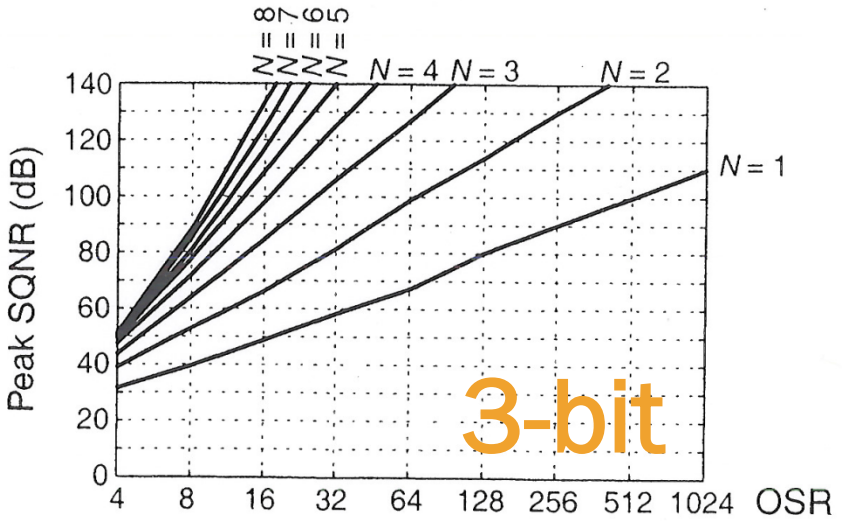
EMPERICAL SQNR LIMITS

- Compare Modulator Order vs. OSR vs. Quantizer Resolution

[Schreier and Temes, 2005]

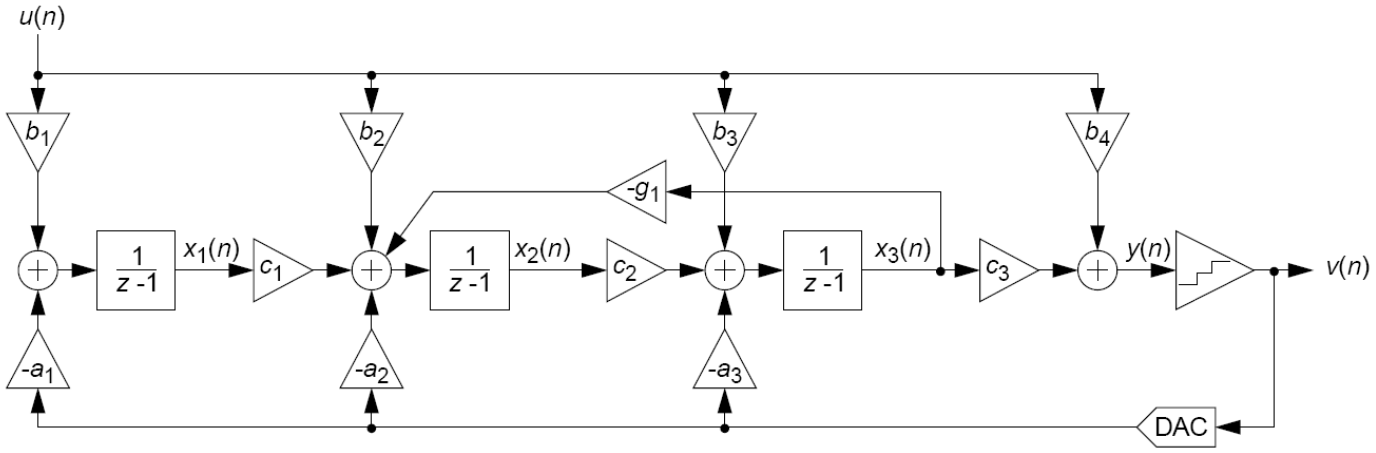






EXAMINE ARCHITECTURE

- Consider ΔΣ Topologies
  - Single Loop vs. MASH; CIFB, CIFF, CRFB, CRFF, etc.



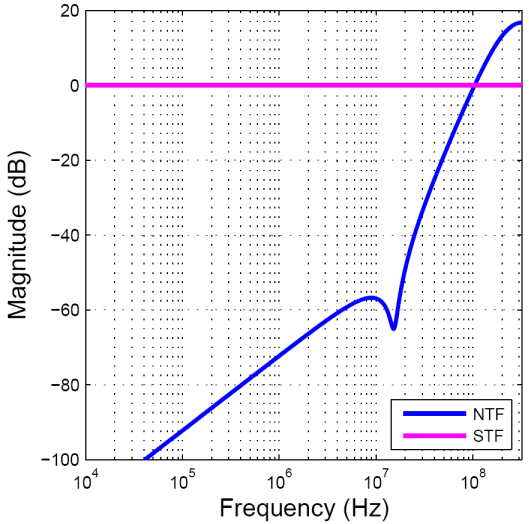
- Write MATLAB script to optimize coefficients
  - Order, OSR, Bits, $\|H\|_\infty$, etc.
  - DStoolbox → dsdemo[1-3].m

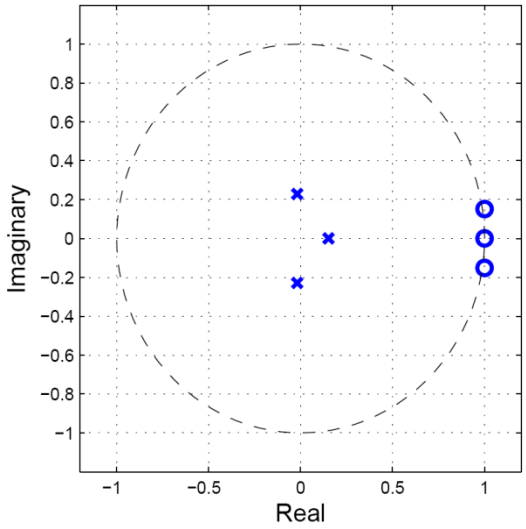
MATLAB SCRIPT OUTPUT

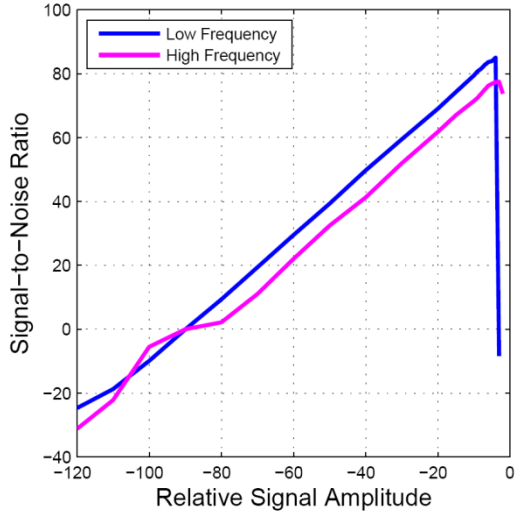
- Modulator Coefficients
- NTF and STF
  - Magnitude
  - Poles and Zeros
- Time-domain Simulation Results

MODULATOR COEFFICIENTS

a_1	2.885522268923101
a_2	2.795275751639167
a_3	0.858455887399655
b_1	1
b_4	1
c_1	1
c_2	1
c_3	1
g_1	0.022954073145617



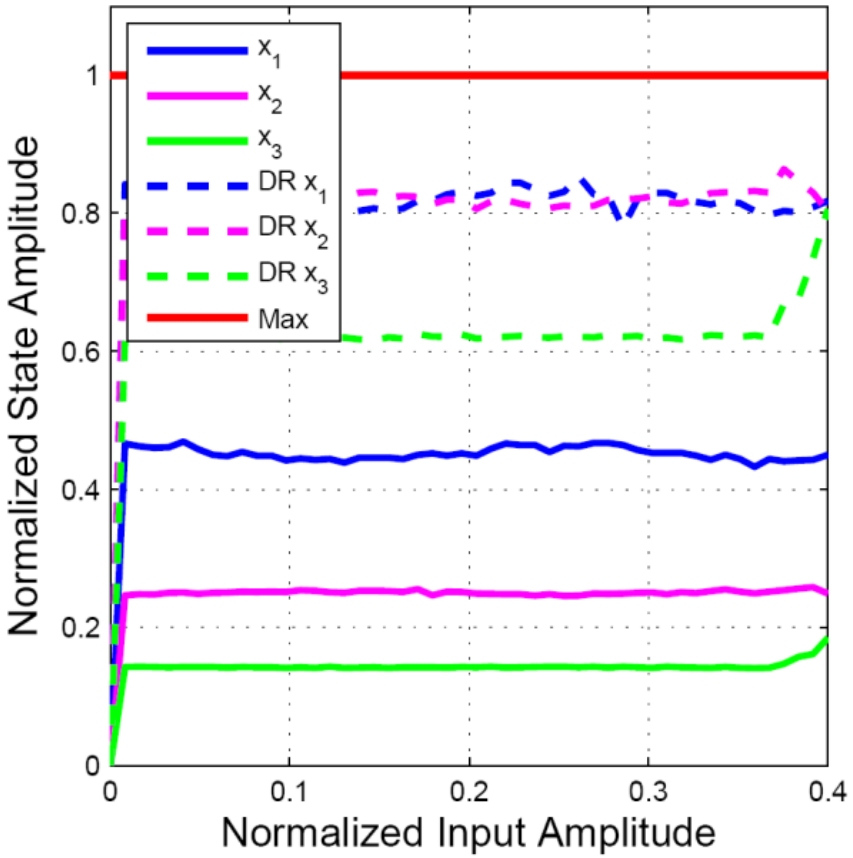




DYNAMIC RANGE SCALING

- Refer to dsdemo3.m
- scaleABCD(, , , $[x_1, ..., x_L]$, , ,)
- xlim = $[x_1, ..., x_L]$
- Iteratively adjust values of *xlim* to change [a, b, c, g] coefficients
- Examine [a, b, c, g] coefficients for integer ratio quantization → *Eases switched-capacitor integrator ratios, and matching*

D.R. SCALING RESULTS



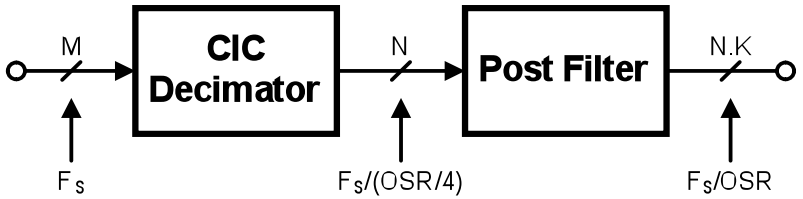
DYNAMIC RANGE SCALED MODULATOR COEFFICIENTS

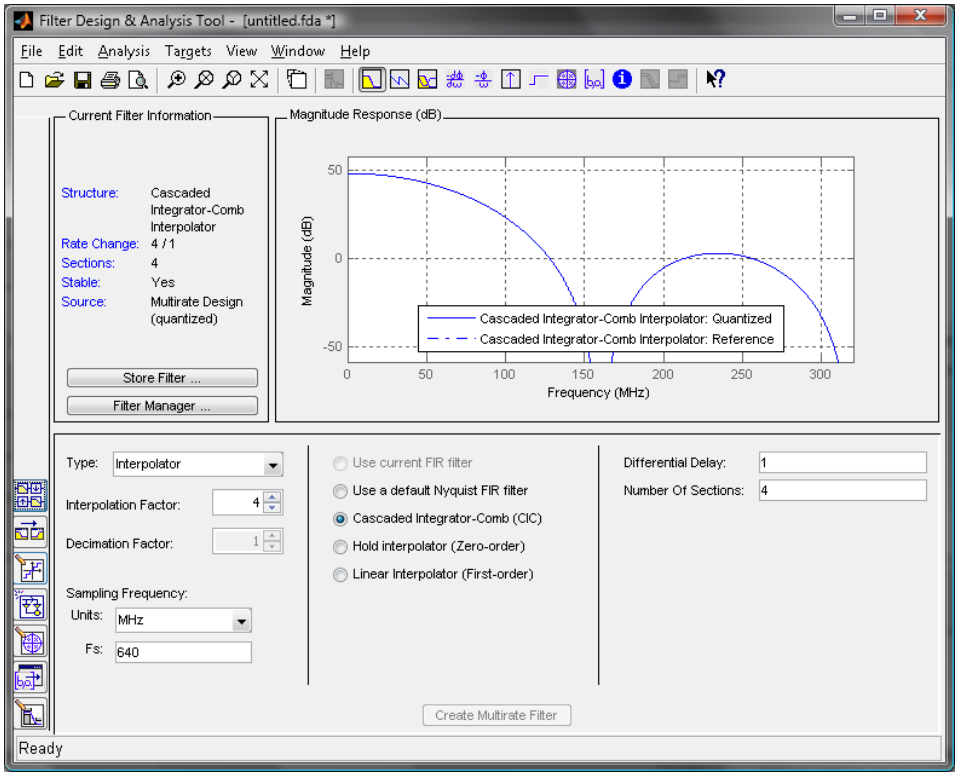
	Full Precision	Quantized
a_1	1.587037247907706	17/11
a_2	0.854112035223079	9/11
a_3	0.196729474195754	2/11
b_1	0.363636363636364	8/22
b_4	0.2	2.2/11
c_1	0.909090909090909	20/22
c_2	1.8	9/5
c_3	1.333333333333333	4/3
g_1	0.017215554859213	1/60

- Maximize State Amplitude to minimize distortion
- Leave some margin

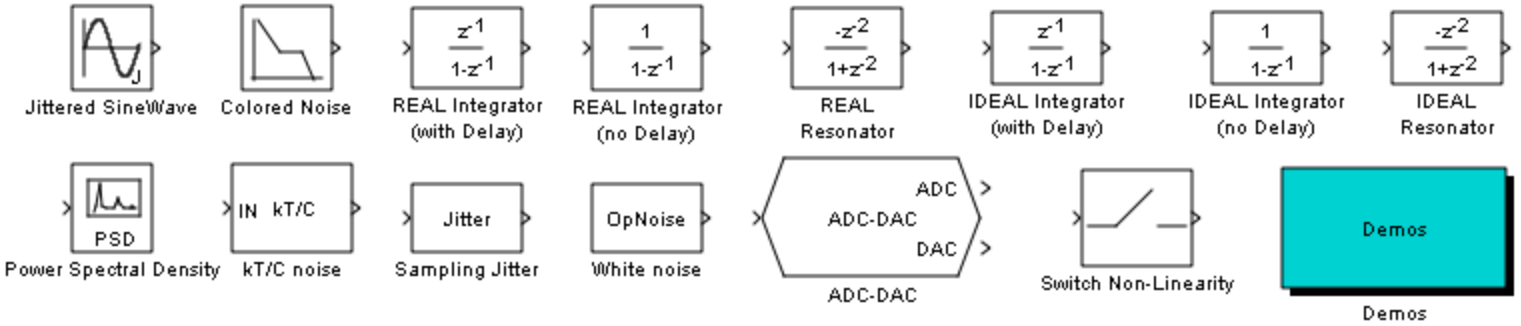
FILTER DESIGN

- MATLAB fdatool
  - Multirate filter (CIC Decimator)
  - Design Post Filter
  - Quantize Coeff.
    - Fixed-point Math
- Export to Script or Simulink



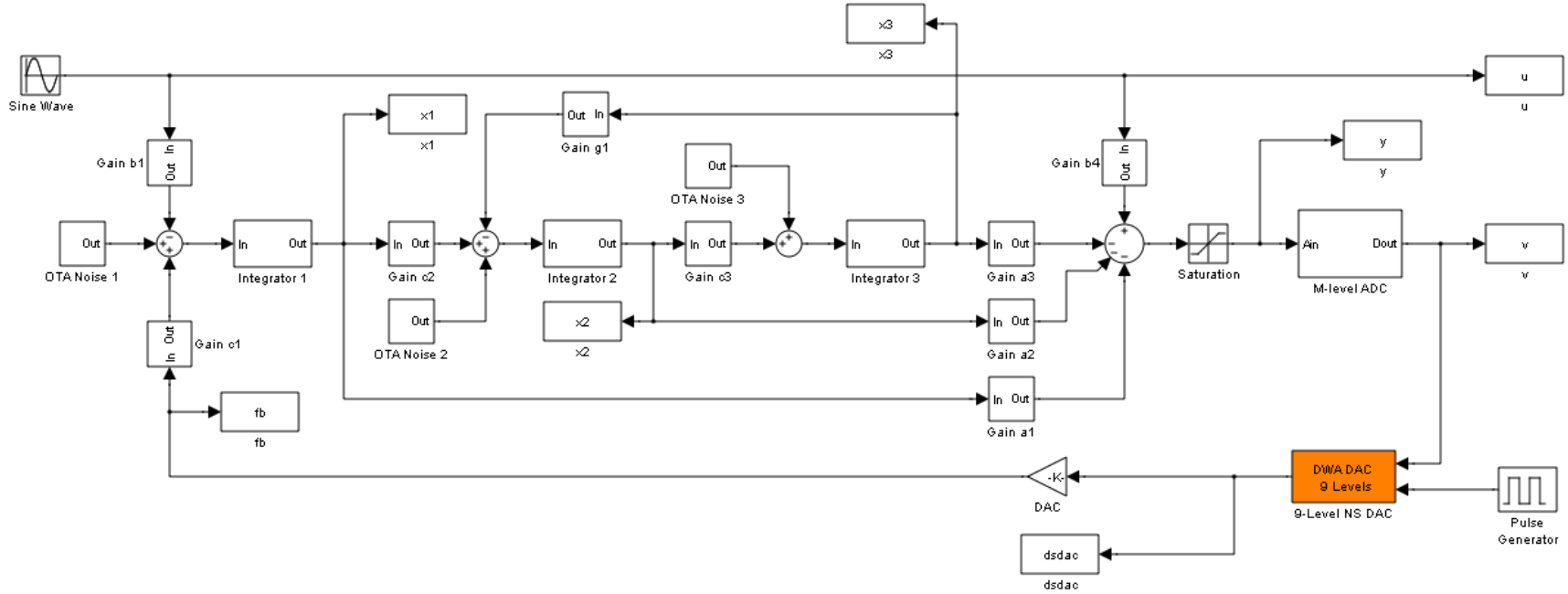


SD TOOLBOX 2 BLOCKS



- Use as starting point
- Noise Sources
  - kT/C Noise
  - White Noise
- Real Integrator
  - Finite Gain
  - Gain Bandwidth
  - Slew Rate

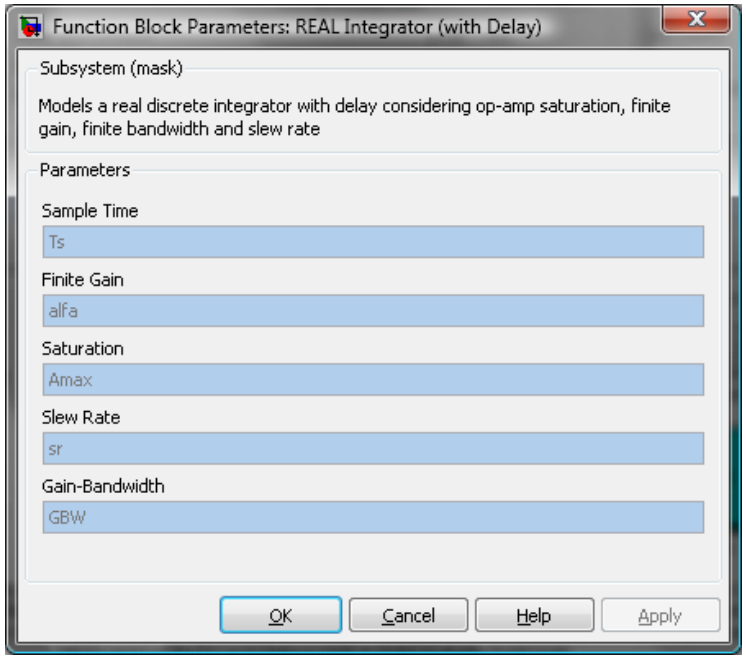
SIMULINK MODEL – 3RD ORDER CIFF



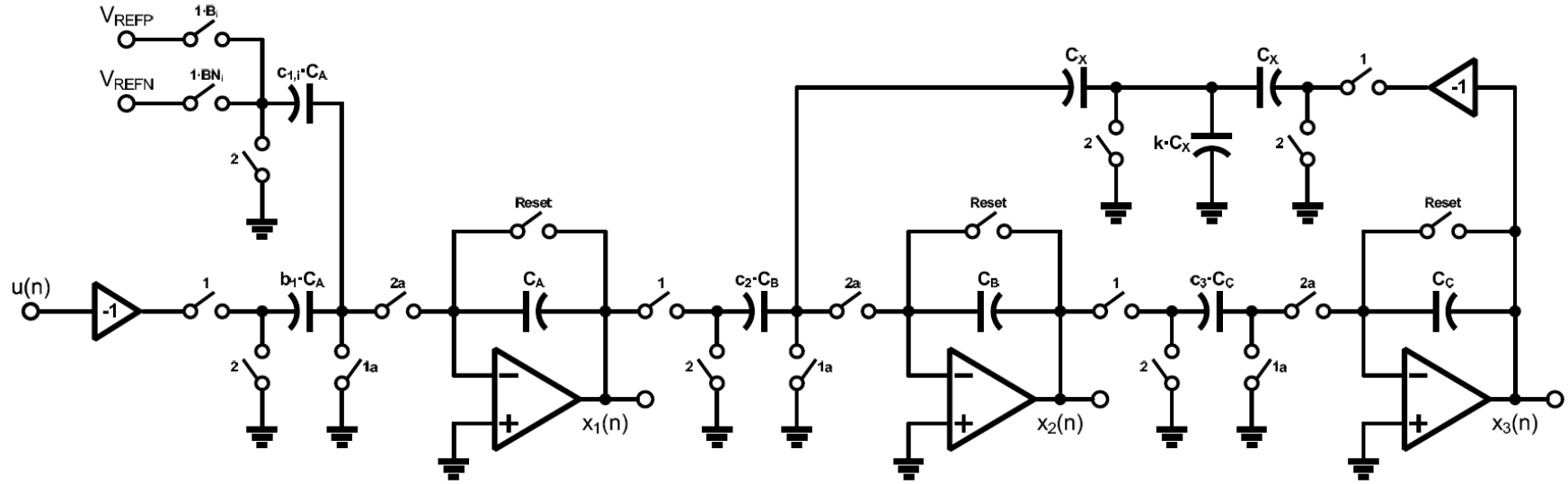
- Finite Gain & BW, SR
- DAC & Cap Mismatch
- Analog Noise
- Digital Round-off Errors
- Create MATLAB script to control Simulink model

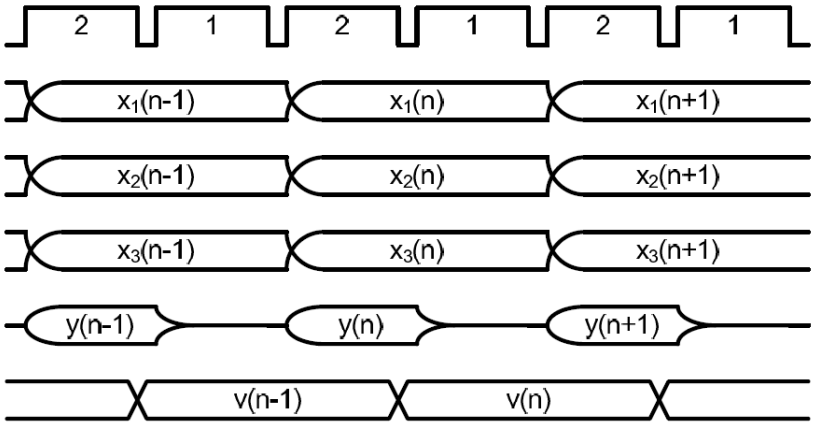
SIMULINK BLOCK & SIMULATION PARAMS

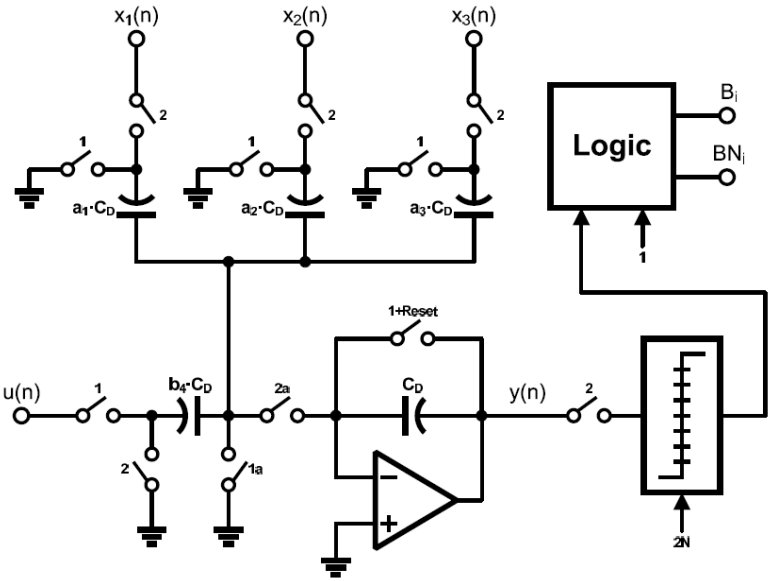
- Initialize variables in MATLAB script
- Choose “Accelerator” to speedup simulation
  - Must have C/C++
- Configuration Parameters → Solver options → variable step, discrete (no continuous states)



SWITCHED-CAPACITOR IMPLEMENTATION

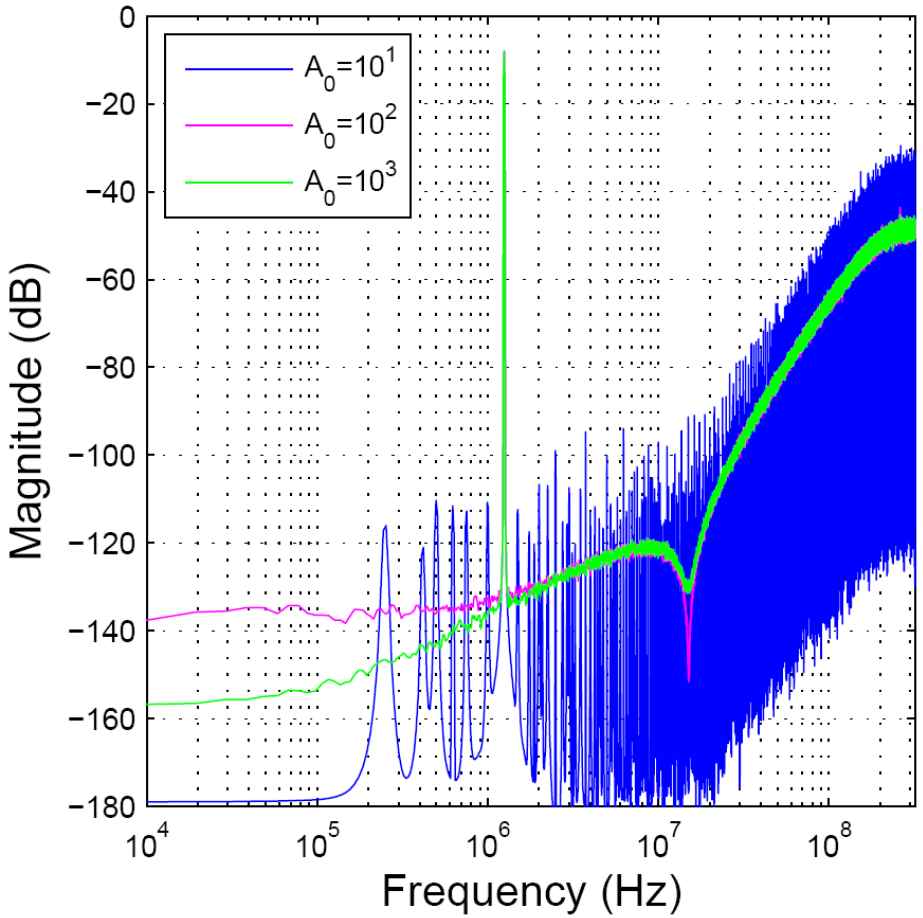






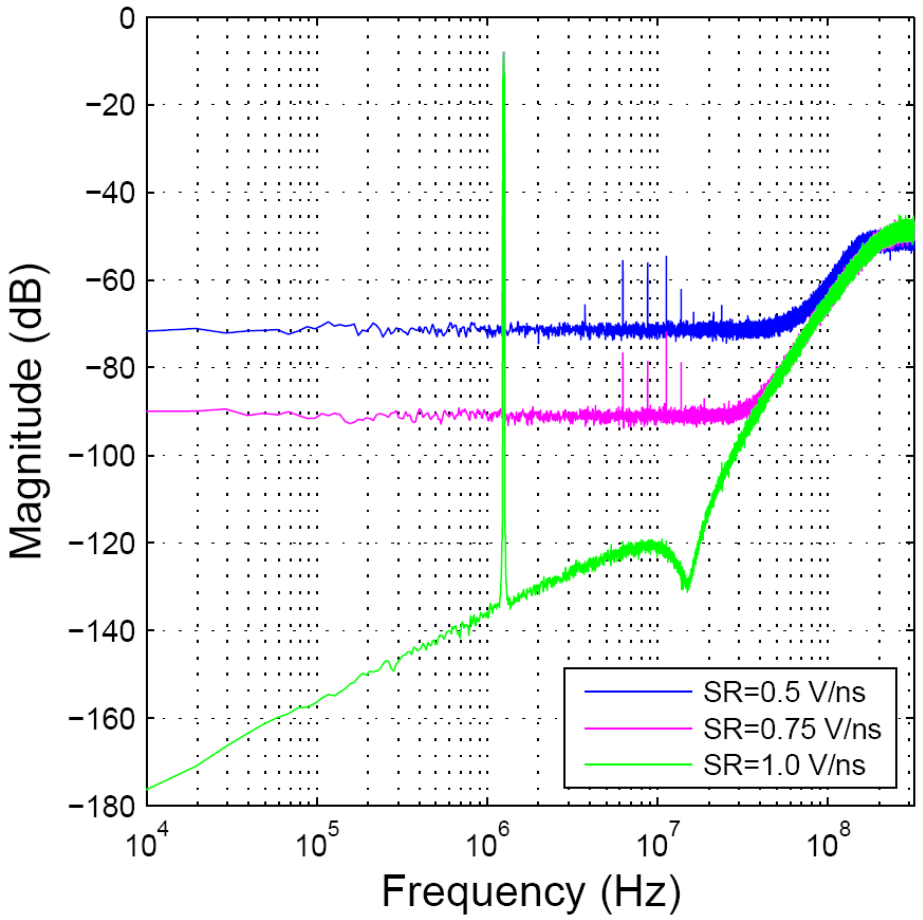
FINITE GAIN – SIMULINK

- Folding of quantization error
- Shifts NTF zero locations



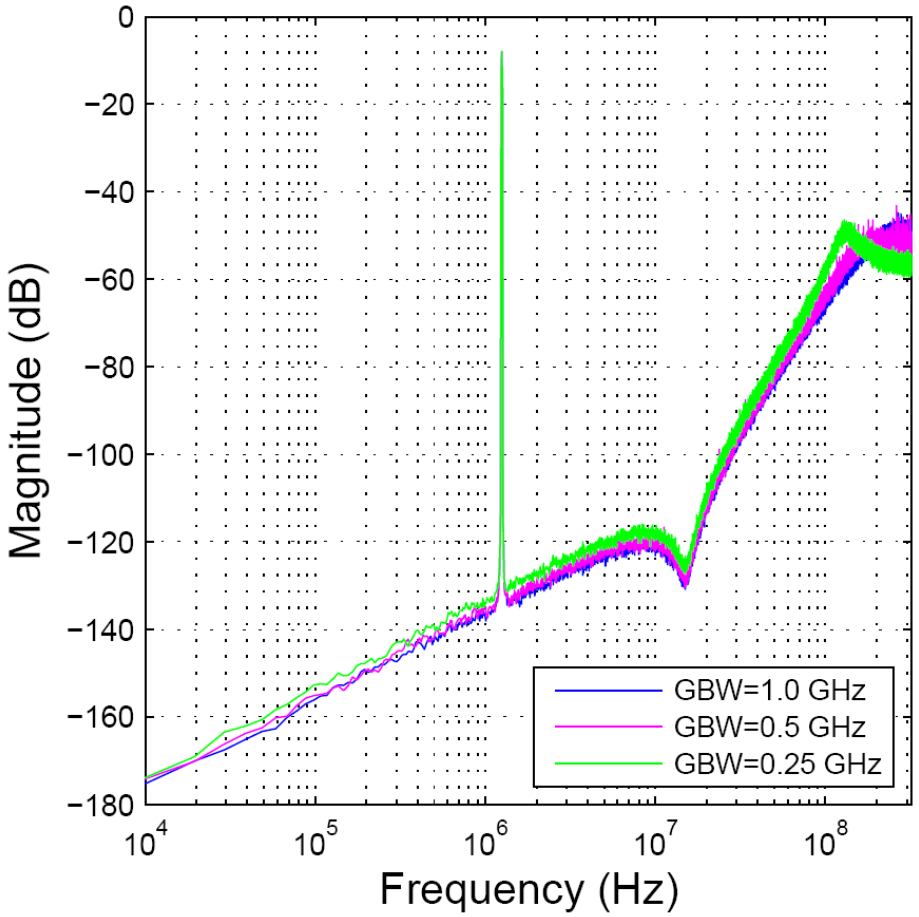
SLEW RATE – SIMULINK

- Based on max integrator step size
- Abrupt impact on integrator settling
- Interdependence with GBW



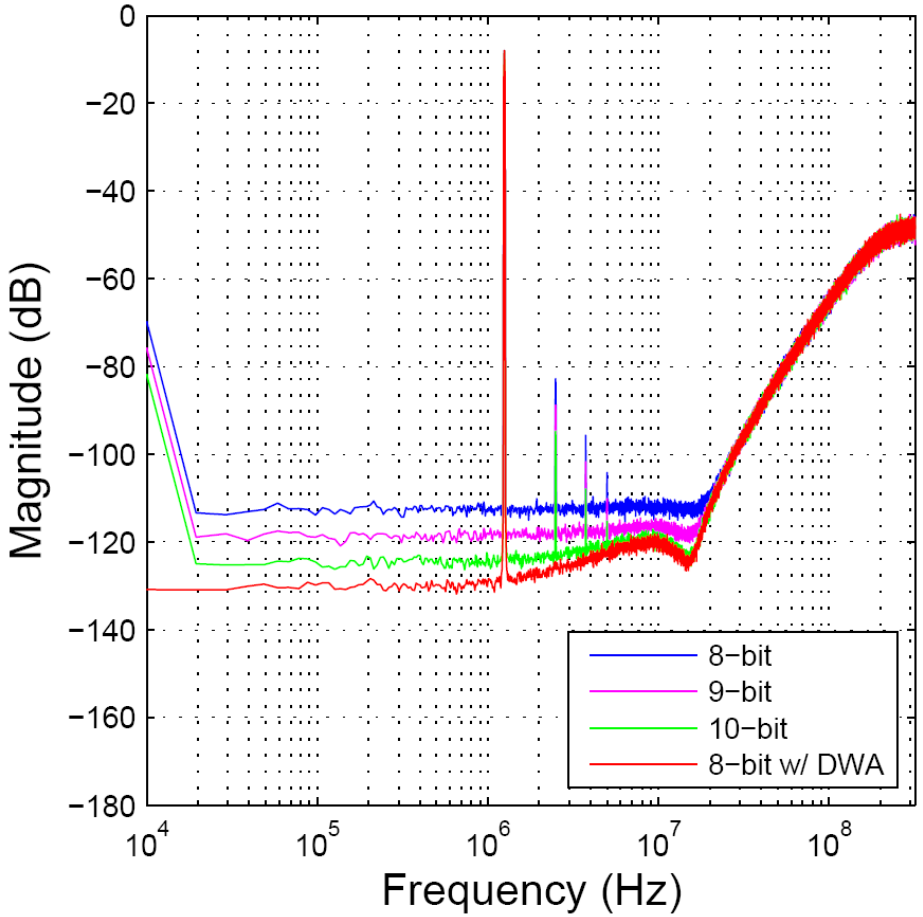
GAIN BANDWIDTH – SIMULINK

- Can cause increased in-band quantization noise
- GBW of the order of F_S
- Interdependence with Slew Rate



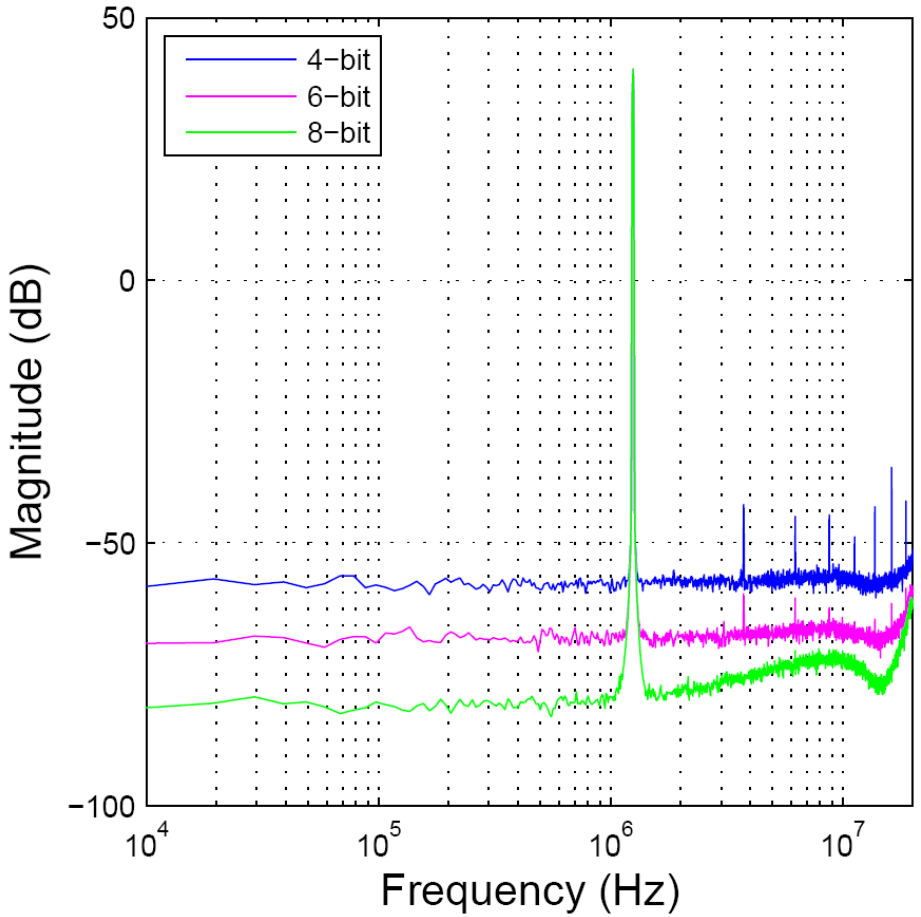
DAC MISMATCH AND DWA – SIMULINK

- Examine dsdemo5.m
- Mismatch causes distortion
- DWA high-pass filters mismatch



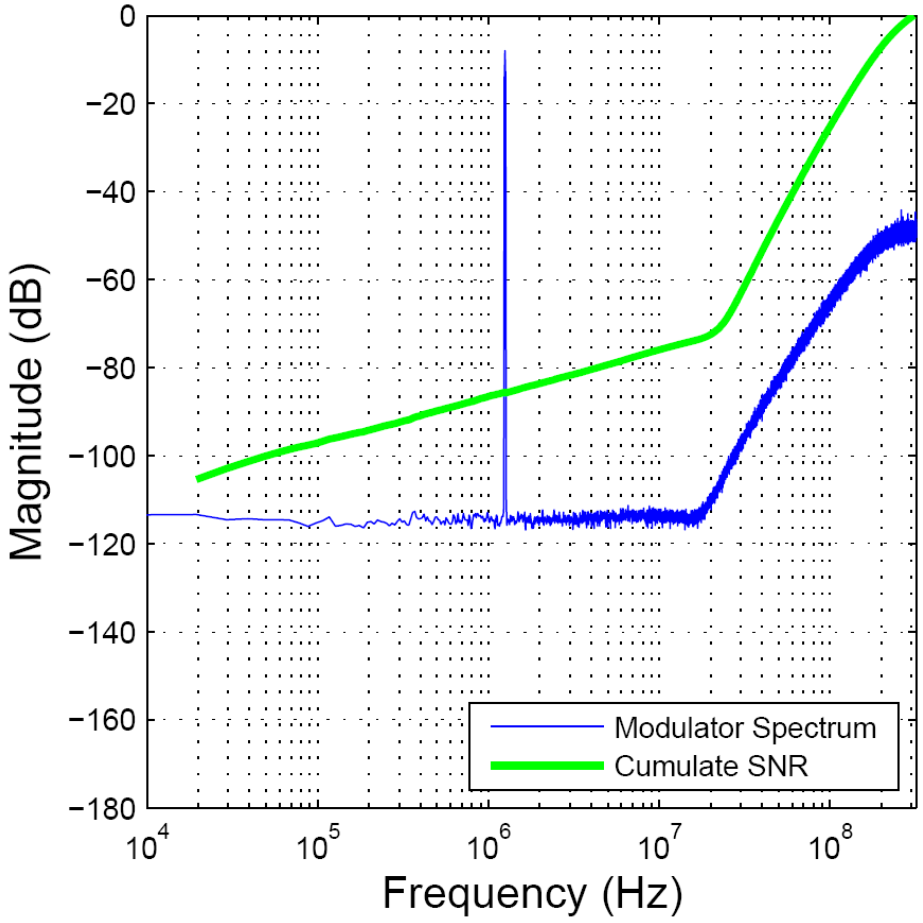
DIGITAL ROUND-OFF ERROR – SIMULINK

- MATLAB fdatool
- Quantize Coeff.
- Internal Precision
- Output Fraction Bits
- Code into MATLAB
  → Easier Testing



MODULATOR SPECTRUM

- Includes non-ideal effects
- DWA active (8-bit matching)
- Average of 32 runs, 2^{16} points
  - Initialize Integrator States Randomly

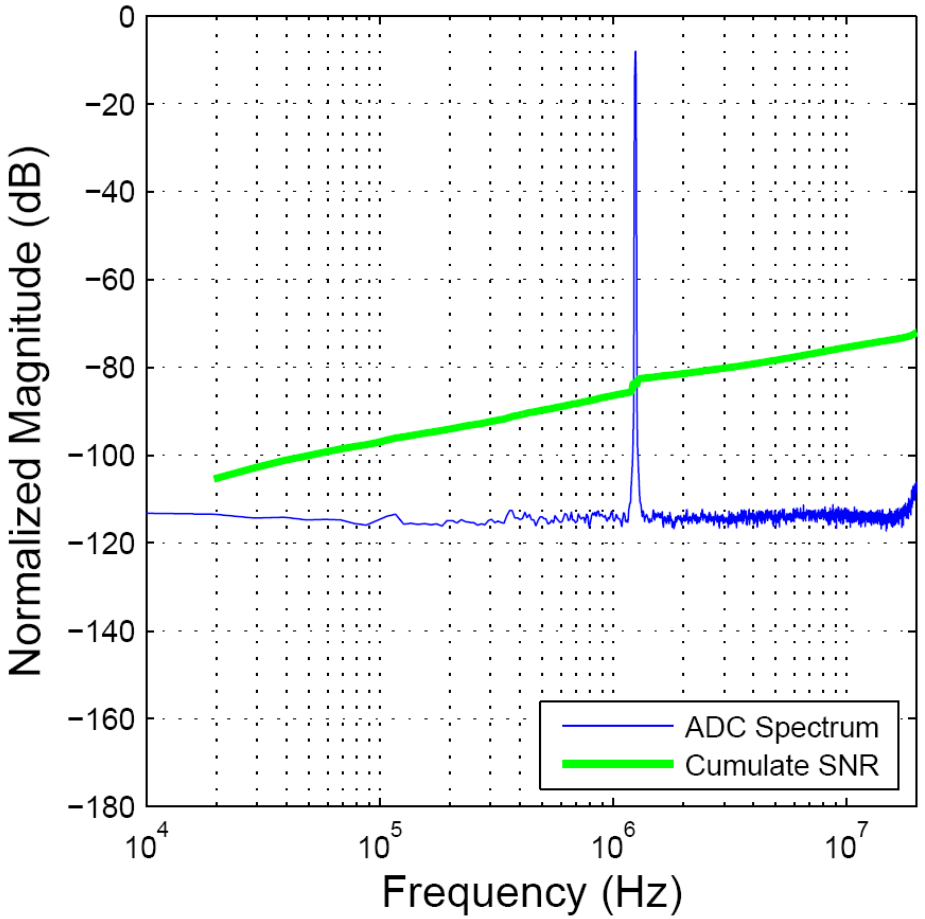


ADC SPECTRUM

- PSD of Decimated and Filtered Output
- F_{BW} = 20 MHz

DESIGN SPECIFICATIONS

Signal Bandwidth	0 – 20 MHz
Clock Frequency	$\leq$ 640 MHz
Min Unit Cap	25 fF
Total Capacitance	6.71 pF
Amplifier DC Gain	100 V/V
Amplifier SR	5.2 V/ns
Amplifier GBW	1.0 GHz
DAC 1-σ	0.39%
Total Word Length	21 bits
Fraction Length	8 bits
ENOB @ 156.25 kHz	11.69 bits
ENOB @ 20 MHz	11.36 bits
Power Supply	1V
Input Signal Range	$\pm 1 V_{diff}$



PROJECT SUGGESTIONS

- *Start Early!*
- Understand DStoolbox dsdemo's
- Write DStoolbox Script
  - *Fully* test before starting Simulink and Cadence!!!
- Build Transistor-based Switches in Cadence
  - Helps mitigate convergence issues
- Understand SD Toolbox 2 (Simulink) and adapt to your system